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(54) Audio signal reproducing apparatus

(57) Audio signal reproducing apparatus comprising a source of audio signals, a plurality of transducers for generating sound from audio signals applied thereto, and transducers being spaced apart within an area, and a switching means to apply audio signals from said source to one or more of the transducers, the particular transducer or combination of transducers to which said signals are applied being varied automatically with time. Switching may involve pre-determined patterns of transducers as in one embodiment, or any mathematically possible combination of patterns of transducers as in another embodiment. Switching may be controlled by manual input 36 or automatic selection 28 of sequences of combinations of transducers with time. Said sequences of combinations may be programmed into a retrieval system such as a microcomputer. The above arrangements provide a switched, moving sound image which may be enhanced by a stable, background stereo arrangement. The output stages OC1 may include an attenuator which may be ramped up or down for smooth transition.

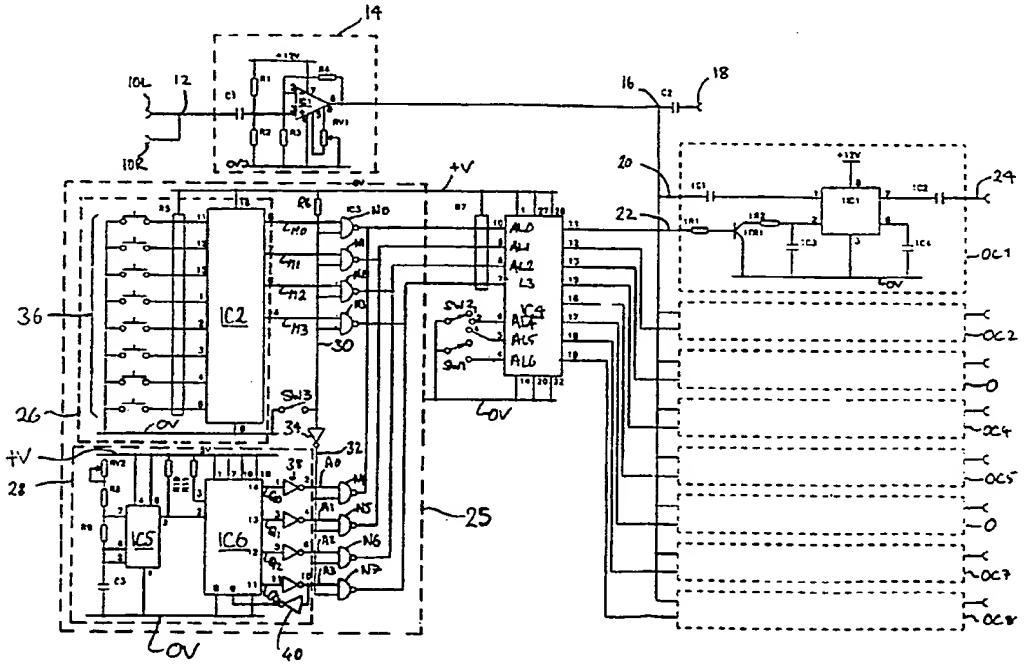

Fig 1

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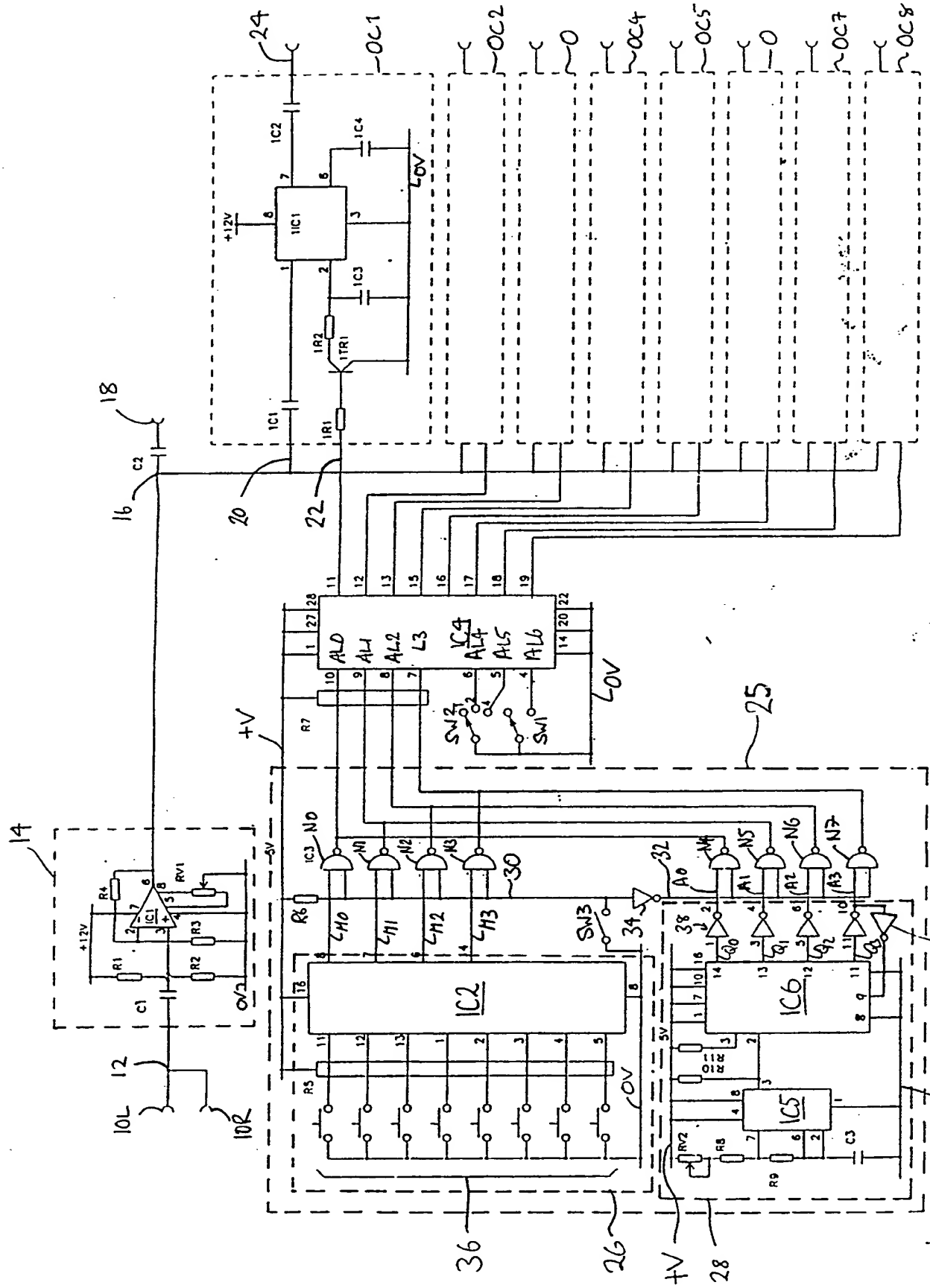
24
OC1
OC2
OC4
OC5
OC7
OC8
18
16
20
22
14
25
+V
0V
10L
10R
12
36
26
28
30
32
34
38
40
IC1
IC2
IC3
IC4
IC5
IC6
SW1
SW2
SW3

FIG 1

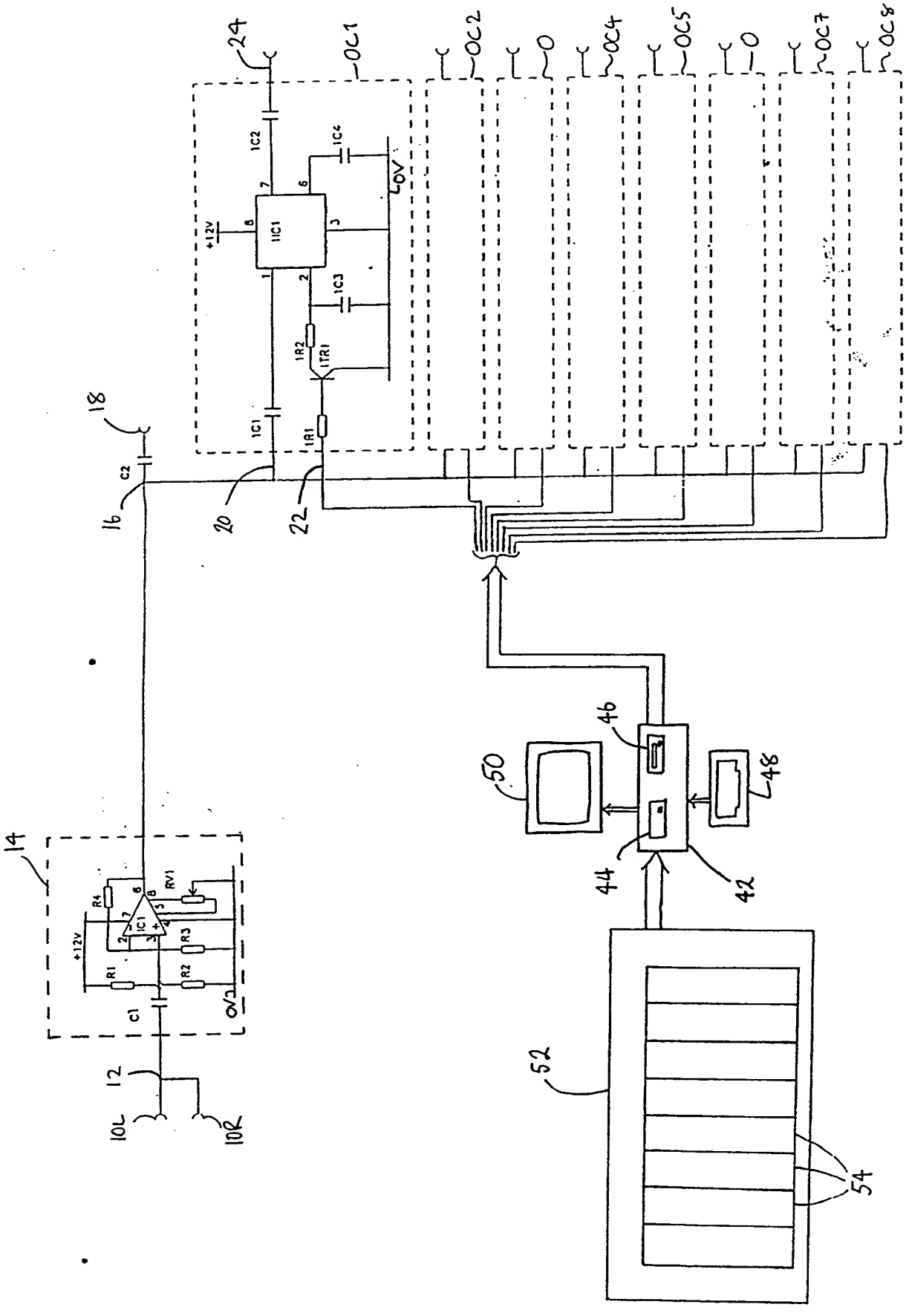
24
OC1
OC2
OC4
OC5
OC7
OC8
IC2
IC4
+12V
0V
IIC1
IC3
IR2
ITR1
IR1
IC1
18
C2
16
20
22
14
RV1
R4
IC1
+12V
R3
R1
R2
C1
0V2
12
10L
10R
46
50
48
44
42
52
54

FIG 2

AUDIO SIGNAL REPRODUCING APPARATUS

The present invention relates to audio signal reproducing apparatus.

Many systems for recording and reproducing audio signals have been proposed which aim to provide more realistic sound reproduction than can be provided by a simple mono system. By far the most common of these is stereo recording and reproduction in which sound is recorded in two separate audio channels and then, typically, reproduced from two spaced apart loudspeakers to generate a substantially two dimensional sound image in which a listener can pick out the positions of individual sounds from a plurality of sounds being simultaneously reproduced.

Stereo recording and reproduction has proved to be extremely successful to the extent that substantially all musical recordings are now produced in stereo. However, there are situations (for example in discotheques and clubs) where a three dimensional sound image is desirable to provide an enhanced effect for the listener.

Hitherto, several systems for producing a three dimensional sound image have been proposed. For example, quadraphonic recording and reproduction uses four independent audio channels, the sound being reproduced, typically, through four speakers placed at the corners of a rectangle. A listener within the rectangle is presented with a three dimensional sound image in which individual sounds can be separately identified. Also known is the Dolby Surround (Trade Mark) system in which a plurality of (typically six) speakers are used to provide an experience of ambient

sound. Typically, a primary stereo signal is fed to two of the speakers while additional speakers to the front and rear of the listener reproduce an ambient component of the sound.

These known systems, however, have several disadvantages. Firstly, they can only produce a three dimensional sound image from a source recording which has been coded in a manner suitable for use with the system. This severely limits the amount of material which can be reproduced satisfactorily using such systems so limiting their appeal. Secondly, particularly in the case of the Dolby Surround system, the reproducing apparatus is complicated and expensive.

The aim of the present invention is to provide a system for reproducing conventional mono or stereo audio recordings in such a manner as to give a three dimensional audio image.

According to a first aspect of the invention there is provided audio signal reproducing apparatus comprising a source of audio signals, a plurality of transducers for generating sound from audio signals applied thereto, said transducers being spaced apart within a listening area, and switching means operative to apply audio signals from said source to one or more of the transducers, the particular transducer or combination of transducers to which said signals are applied being varied automatically with time by said switching means.

Through careful placement of the transducers (which may typically be loudspeakers) within the listening area, the effect of the operation of the

switching unit is to cause the apart source of the sound to move within the listening area.

Typically the source of audio signals will generate a stereo pair of audio signals. In such circumstances, the stereo pair is preferably combined to form a mono signal representing the sum of the stereo pair before being fed to the switching means. This arrangement ensures that the whole audio signal is processed by the switching means and heard by the listeners. In such arrangements each of the stereo pair of signals is preferably individually applied directly to a respective further transducer. This can enhance the sound received by the listener by providing a stable background to the switched, moving sound image.

In a first embodiment, the switching means may be operative to switch the signal between the transducers in simple, pre-determined patterns. For example, assuming that the transducers are numbered 1, 2, 3....n, the switching unit may apply the signals to the transducers in sequential order, starting at 1 again once n has been reached. Alternatively, (for systems where n is even), the signal may be applied to transducer 1, then $\frac{1}{2}n$, then 2, then $\frac{1}{2}n + 1$ and so on. If the transducers are arranged in order around the periphery of a listening area, these sequences give the impression, respectively that the sound is moving around the area that it is following a zig-zag course across the area.

In the embodiment described above, the signals may be applied to each transducer in turn individually. Alternatively, the signal may be applied to, for example, a pair of neighbouring transducers, to

oppositely-disposed transducers, or to any other combination of transducers.

Preferably, the order of application and the combination of transducers to which the signals are applied are selectable by an operator.

In a second embodiment, the switching means may be operative to switch the signal between the transducers in a pre-programmed sequence. In such an embodiment, the switching means preferably comprises a program storage means operative to store and execute sequences of instructions for control of the switching means. Conveniently, the program storage means may comprise a microcomputer.

In this embodiment, the program storage means is preferably provided with manual input means through which a sequence of switching operations may be input by a user and stored by the program storage means for later execution. Such input means may conveniently comprise a plurality of switches, each switch corresponding to a respective transducer, operation of a switch being recorded by the program storage means as an instruction to apply the audio signal to the corresponding transducer.

Preferably (in either of the above embodiments) the switching means comprises an input connected to the source of audio signals, a plurality of outputs each connected to a respective transducer, and, for each output, a switching circuit operative upon receipt of a control signal to connect the corresponding transducer to the input and on removal of the input signal to disconnect the corresponding transducer from the input. Preferably, the switching circuits are operative to

cause the connection and disconnections to occur in a ramped manner. That is to say, connection is made initially in a highly attenuating mode, the attenuation then, over time, being lowered to a minimum, and disconnection is made in the opposite manner. This is desirable to ensure that the sound image moves in a smooth, non-jerky manner.

From another of its aspects, the invention provides a method of reproducing audio signals in which an audio signal is applied to one or more of a plurality of transducers for reproduction, the transducer or transducers to which the signal is applied being varied automatically with time.

Embodiments of the invention will now be described in detail, by way of example, with reference to the accompanying drawings in which:-

Figure 1 is a circuit diagram of a switching means of a first embodiment of the invention; and

Figure 2 is a circuit diagram of switching means of a second embodiment of the invention.

An audio signal reproducing apparatus embodying the invention comprises a source of audio signals, such as a CD player, the output of which comprises a stereo pair of audio signals.

In the present embodiment each of the signals is fed through amplification means to a respective loudspeaker. The amplification means may conveniently be constituted by the channels of a stereo amplifier. These loudspeakers are driven by the source

continuously to form a stereo background to the audio output.

The sum of the pair of signals (a mono signal) is in addition fed through a second amplification means to a switching means. Each switching means has a plurality of (for example, eight) outputs each of which is connected to a respective loudspeaker.

In a first embodiment of the invention, the switching means comprises a circuit illustrated in Figure 1.

With reference to Figure 1, the switching means comprises a pair of input connectors 10L, 10R, to which are fed, respectively, the outputs of the second amplification means for the left and right audio signals of the stereo pair. Within the switching means, the signals are combined to form a mono signal at point 12.

From point 12, the audio signal is fed to an input stage 14. The input stage 14 comprises an operational amplifier operating in non-inverting mode. The gain of the operational amplifier is chosen (by a selection of suitable values for a feedback resistor R4 and resistor R3, as shown in Figure 3, in a manner well known to those skilled in the art) such that its output provides a signal at a level suitable for further processing as will be described below.

A variable resistor RV1 is connected to the operational amplifier RC1 and to the zero-volt supply line OV, by means of which any variation in output from the operational amplifier RC1 may be compensated.

The output from the input stage 14 is fed to a point 16. A capacitor C2 is connected to the point 16 and to an auxiliary output connector 18. Additional apparatus for processing the signal (such as further switching means to allow further loudspeakers to be driven by the system) may be connected to the auxiliary output connector 18.

From point 16 the audio signal is fed to eight identical output channel stages 0C1 to 0C8, the operation of which will be described below.

In Figure 1, the circuit of output channel stage 0C1 is shown in detail. The other output channel stages 0C2 to 0C8 have identical circuits and the description of output channel stage 0C1 thus applies equally to these other output channel stages.

Output channel stage 0C1 has a signal input 20 to which is fed the audio signal emanating from point 16. The output channel stage 0C1 also has a control input 22. The signal input 20 is connected through a capacitor 1C1 to an audio attenuator integrated circuit 1IC1. The output from the attenuator 1IC1 is fed through a capacitor 1C2 to a signal output 24.

The control input is connected through a resistor 1R1 to the base of a transistor 1TR1. The emitter of the transistor 1TR1 is connected to the zero-volt line 0V while its collector is connected through a resistor IR2 to a control pin of the attenuator 1IC1. The control pin is also connected through a capacitor IC3 to the zero-volt line 0V.

In operation, the level of attenuation of 1IC1 is controlled by the voltage on its control pin while the

control output 22 to the output channel stage OC1 remains high (the inactive state) the control pin of 1IC1 is connected to the zero-volt line OV through the resistor IR2 and the transistor 1TR1. Also, the capacitor IC3 is maintained in a discharged state. When the control input 22 goes low, the transistor 1TR1 switches off. This allows the capacitor IC3 to be charged by the attenuator 1IC1 through its control pin, so causing the voltage on the control pin to rise. As the voltage rises, the attenuation diminishes and so the audio signal appearing at the signal output 24 increases. Thus, the application of a low voltage to the control input 22 of an output channel stage OC1 to OC8 causes the audio signal to be applied to the loudspeaker connected to that output channel stage OC1 to OC8.

The switching means further comprises an EPROM IC4 of 8192x8 configuration. Each data line D1 to D8 of the EPROM IC4 is connected to the control input 22 of a corresponding output channel stage 0C1 to 0C8. The address lines A0 to A6 of the EPROM IC4 are connected as follows:

The least significant four address lines AL0 to AL3 are connected to the output of an address generating stage 25 to be described below.

Address line AL6 is connected to one output terminal of a single-pole two position switch SW1, the input terminal switch being connected to the zero volt line OV. The other output switch SW1 is open circuit. Address lines AL4 and AL5 are, respectively, connected to first and second outputs of a single-pole three position switch SW2. The input to the switch SW2 is

connected to the zero volt line OV and the third output terminal is open circuit.

The address generating stage 25 comprises a manual address generating sub-stage 26 and an automatic address generating sub-stage 28. The manual address generating sub-stage 26 comprises four output lines M0 to M3 and the automatic address generating sub-stage has four output lines A0 to A3. The output lines M0 to M3 of the manual address generating stage are each connected to a first input of a respective two-input NAND gate N0 to N3. The second input of each of these NAND gates N0 to N3 is connected to a common line 30 which is, in turn, connected to the five volt line +V through a resistor R6. The output of each NAND gate N0 to N3 is connected to a respective output of the address generating stage 25.

The four outputs A0 to A3 of the automatic address generating sub-stage 28 are similarly connected to a respective NAND gate N4 to N7, the outputs of which are connected to the outputs of NAND gate N0 to N3 respectively and then to the output of the address generating stage. The second input of each NAND gate N4 to N7 is connected to a second common line 32. The second common line 32 is driven by the first common line 30 through an invertor 34.

A switch SW3 is connected between the first common line 30 and the zero volt line 0V.

In operation, when the switch SW3 is open, the first common line 30 is pulled up to five volts by virtue of its connection through the resistor R6 to the five volt line +V, so causing the second input of the NAND gates N0 to N3 to become high. The output to

each of the NAND gates N0 to N3 is, therefore, the complement of the signal on their first input - that is to say it is the complement of the value on the output lines M0 to M3 of the manual address generating sub-stage 26. The output of the invertor 34 drives the second common line 32 to the low state. Thus, the output of the NAND gates N4 to N7 is high irrespective of the condition of their first inputs.

If, on the other hand, switch SW3 is closed it will cause the first common line 30 to be pulled down to a low state. Thus, the second input to each of the NAND gates N0 to N3 is also in the low state causing their outputs to be high, irrespective of the condition of their first inputs. The output of the invertor 34 is high, so driving the second common line 32 high, which in turn causes the second input of each of the NAND gates N4 to N7 to go high. Thus the output of each of these NAND gates is a complement of the value of its first input line, which is determined by the outputs A0 to A3 of the automatic address generating sub-stage 28.

Thus, while the switch SW3 is open, the output of the address generating stage 25 is determined by the output of the manual address generating sub-stage 26, and when switch SW3 is closed the output of the address generating stage 24 is determined by the output of the automatic address generating sub-stage 28.

The manual address generating sub-stage 26 comprises an address encoder IC2 having eight input lines each connected to the positive supply line through a pull-up resistor R5 (R5 is a resistor pack containing eight resistors). Each of the input lines is also connected through a respective normally-open push

button switch (the switches being indicated generally at 36) to the zero volt line 0V. Thus, each input line is at a high voltage state until the corresponding switch 36 is depressed, whereupon it is pulled down to zero volts.

The encoder IC2 also has four output lines which constitute the output lines M0 to M3 of the manual address generating sub-stage. The encoder IC2 generates on its output lines a binary representation of the state of its input lines. Thus when all input lines are in a high state (that is, none of the push buttons 36 pressed) all output lines will be in a high state representing a complementary inversed binary value zero. If one of the switches 36 is pressed then the output lines will adopt, high and low states to represent a number between 1 and 8, thus identifying the switch 36 which has been pressed.

The automatic address generating sub-stage 28 comprises a synchronous counter IC6 and a timer IC5. In this embodiment, the timer IC5 is the well known 555 IC. IC5 is connected as follows:

Pins 1 and 8 (power supply) are connected, respectively to the zero volt and five volt lines OV, +V. Pin 4 (reset) is also connected to the five volt line +V so that the timer runs continuously. Pins 2 and 6 are together connected to the first side of a capacitor C3, the other side of which are connected to the zero volt line OV. The first side of C3 is also connected to the five volt line +V through resistors R9 and R8 and variable resistor RV2 connected in series. The wiper of RV2 is connected between RV2 and R8. Pin 7 of the IC is connected between R8 and R9. Thus, IC5 produces at its output pin 3 a continuous chain of

separate, regular pulses, the frequency of which depends upon the setting of RV2.

The output of the timer IC (which is connected to the five volt +V line by a resistor R10) is fed to the clock input of the counter IC6. In this embodiment, the counter is conveniently implemented by using a 74162 IC. The counter IC6 has its power supply (pins 8 and 16) connected conventionally to the zero volt and five bolt supply lines 0V, +V Pin 1 (clear) and pins 7 and 10 (enable) are connected directly to the five volt line to ensure that the counter runs continuously. The clock input (pin 2) is connected to the output of the timer IC5. The least-significant bit of the data input lines (pin 3) is connected permanently to the five volt line +V through a resistor R11, while the remaining data input lines are connected to the zero volt line OV. Each output (pins 11 to 14), indicated as Q0 to Q3 in Figure 1, is connected to a corresponding invertor, indicated generally as 38, the output of these invertors constituting the four output lines A0 to A3 of the automatic address generating sub-stage 28. The output of the invertor 38 which is attached to the most significant output line Q3 is fed to the input of an invertor 40, the output of which is fed to the load input (pin 9 of the counter IC6.

The sequence of operation of the automatic address generating sub-stage 28 is as follows:

The timer IC5 generates a continuous chain of pulses on its output which is fed to the clock input of the counter IC6 causing it to count continuously. The counter will continue to increment the number upon its output until its output represents, in binary, a value

of 8 (Q3 high and Q0 to Q2 low). The signal on Q3 is fed through invertor 38 and 40 so upon reaching this output value a positive-going step is fed into pin 9 (load) so that the data input (which is permanently set at binary value 1) is stored in the internal register of the counter IC6. Therefore when the next clock pulse is received from the timer IC5, the output reverts to a value of 1 and the counting sequence resumes. It can thus be seen that the output from the automatic address generating sub-stage 28 on lines A0 to A3 is a sequential, repeating binary representation of numbers 1 to 8, a high voltage level representing binary 0.

To summarise, the output of the address generating stage 25, when switch SW3 is open, is a binary number between 0 and 8, 0 indicating that none of the push buttons 36 is pressed and any other value indicating that one of the push buttons 36 is pressed, or, when switch SW3 is closed, a sequence of binary numbers counting from 1 to 8 and then repeating, the rate of counting being controlled by the setting of variable resister RV2.

The output from the address generating stage 25 constitutes the four least significant bits of an address fed to the EPROM IC4. The three most significant bits are determined by the positions of switches SW1 and SW2.

The value of the data stored in the EPROM IC4 is such that in all cases where the least significant address lines A0 to A3 are all 0 the data is 0. In other cases, where the value in address lines A0 to A3 represents a binary value N ($1 < N < 8$), the data will be such that output data line N is active. Depending

upon the position of switches SW1 and SW2 (and therefore the state of the most significant address lines A4 to A6) other data lines may also be active. for example, a line adjacent to line N or a line "opposite" Line N, in terms of the loudspeaker to which is is connected. It will be understood that to control the output channel stages OC1 to OC8, a binary value of 0 is indicated by a high voltage level on the data line of the EPROM IC4. The effect of this is to cause output channels to be selected principally on the value of the address generating stage 25.

To summarise the operation of this embodiment, when switch SW3 is open, an operator can manually select which of the eight output channels is to be fed with an audio signal by means of the push button switches 36. When switch SW3 is closed, the switching operation takes place automatically under the control of the automatic address generating sub-stage 28. The speed at which the switching takes place can be varied by the operator by means of RV2. Additional effects can be generated in dependence upon the position of the switches SW1 and SW2.

The second embodiment of the invention will now be described with reference to Figure 2. The second embodiment comprises a source of audio signals, a switching means, and a plurality of loudspeakers, all arranged as in the first embodiment. The switching means comprises an input stage 14 and output channel stages OC1 to OC8, also arranged as described above.

The second embodiment further comprises a microcomputer 42 which constitutes a programme storage means. The microcomputer 42 may conveniently be a standard personal computer having a hard disc drive 44

and the floppy disc drive 46. Conventional input/output devices may also be provided such as a keyboard 48 and a visual display unit 50.

The microcomputer 42 has an eight-channel parallel output port which, on a conventional personal computer, may conveniently be constituted by a parallel printer port. Each channel of the parallel port is connected to the input control line 22 of a corresponding output channel stage OC1 to OC8. In this way, data placed on the output port may be used to control the output channel stage OC1 to OC8 by driving their control inputs. For example, if the binary representation of the value 2 is placed on the output port, the input line 22 of the second output channel stage OC2 will be driven low while the control inputs 22 of the remaining output channel stages will be high. Thus, output channel stage 2 will cause an audio signal to be supplied to its corresponding loudspeaker, while all other output channel stages will be switched off.

A data file is stored on the hard disc 44 of the microcomputer 42 which contains a sequence of binary values representing the switching sequence of the various output channel stages OC1 to OC8. In use, the microcomputer 42 executes a program which reads data from the file sequentially and outputs it through the parallel port. The data file may contain further information, for example specifying the rate at which data is to be output, which is read by the program. The program may contain additional function features, for example to allow the user to start the action of the system accurately in synchronism with the start of an audio programme.

The data file may be loaded onto the hard disc 44 into two ways. A user may be supplied with a file produced by a supplier on a floppy disc which is inserted into the floppy disc drive 46 and copied onto the hard disc 44. Alternatively, a new file may be generated as will be explained below.

In order to allow generation of new files, the system may further comprise a switch unit 52. The switch unit comprises a plurality of normally open push switches 54, which may conveniently be laid out in an arrangement resembling an electronic organ keyboard, each switch corresponding to a respective output channel.

The switch unit 52 may be operable to generate an 8-channel output which is sent to a parallel input port of the microcomputer 42, each channel being driven by a high or a low voltage state depending upon the state (pressed or released) of a corresponding switch 54. However, many conventional microcomputers are only provided with serial input ports and for operation of the switch unit 52 with such microcomputers, there may be provided within the switch unit 52 a convertor (such as may conveniently be implemented by means of a UART circuit) which converts the 8-channel parallel data on the status of each switch to a serial representation for onward transmission to the microcomputer 42.

In order to generate a data file, a program is executed which periodically reads values from the input port. In time with the audio programme, a user presses the push button switches 54 which correspond with the particular channels to be activated. The sequence of push presses is stored by the program as a sequence of data read from the input port. This data may

subsequently be fed to the output port to generate a sequence of control signals of the output channels.

The system may, optionally be supplied to end users without the switch unit 52 and without the program for reading data therefrom, the end user relying on data files provided by a manufacturer specifically designed to accompany a particular audio programme.

CLAIMS

1. Audio signal reproducing apparatus comprising a source of audio signals, a plurality of transducers for generating sound from audio signals applied thereto, said transducers being spaced apart within a listening area, and switching means operative to apply audio signals from said source to one or more of the transducers, the particular transducer or combination of transducers to which said signals are applied being varied automatically with time by said switching means.

2. Sound source according to Claim 1 which may be live, pre-recorded, or broadcast in origin.

3. Apparatus according to Claims 1 and 2 in which through placement of the transducers (which may typically be loudspeakers) within the area, the effect of the operation of the switching unit is to cause the apart source of the sound to move within the listening area.

4. Apparatus according to Claims 1-3 in which the source of audio signals will generate at least a stereo pair of audio signals.

5. Apparatus according to Claim 4 in which the at least a stereo pair of signals is combined so as to form a mono signal representing the sum of the at least stereo pair of signals before being fed to the switching means. This arrangement ensures that the whole audio signal is processed by the switching means and heard by the listeners. In such arrangements each of the at least stereo pair of signals is preferably applied directly to a respective further transducer. This can enhance the sound received by the listener by providing a stable background to the switched, moving sound image.

6. In one embodiment, the switching means may be operative to switch the signal between the transducers in single pre-determined patterns. Assuming the transducers are numbered 1, 2, 3 .... n, the switching unit may apply the signals in sequential order, starting at 1 again once n has been reached.

7. According to Claims 1 to 6, the pre-determined patterns may be of any sequence of 1 to n, as long as a pattern is obvious because of a repetative nature.

8. According to Claims 1 to 7, these patterns can be applied to sequences of individual transducers, however these patterns can also be applied to more than one transducer simultaneously. The only restriction here being the number , n, which represents the total number of transducers in the system.

9. According to Claims 1 to 8 the only restriction arising being the mathematical limit of combinations of the number , n, of transducers whether singular or multiple in application. (That is when 1, more than 1, or all up to the limit n, of transducers are figures in the calculation of mathematical possibilities of combinations).

10. Apparatus according to all previous claims in which the order and the combination of transducers to which the signals are applied are selectable by an operator.

11. In another embodiment, the switching means may be operative to switch the signal between the transducers in a pre-programmed sequence. In such an embodiment, the switching means preferably comprises a program storage means operative to store and execute sequences of instructions for control of the switching means. Conveniently the storage means may comprise a microcomputer.

12. According to Claim 11, the program storage means is preferably provided with manual input means through which a sequence of switching operations may be input by a user for simultaneous execution and stored by the program storage means for later execution as and when the sequence is required.

13. According to Claims 11 and 12, such input means conveniently comprising a plurality of switches, each switch corresponding to a respective transducer, operation of a switch being recorded by the program storage means is an instruction to apply the audio signal to the corresponding transducer.

14. According to Claim 13 whereby more than one switch can be operated simultaneously up to the limit n. n in this case corresponding to the number of transducers as well as the number of switches. The only mathematically limiting factor in switch operation and subsequent recording by the program storage means being the total number of mathematical combinations of the number , n, of transducers, each of which has a corresponding switch for input into the storage means. The only limiting factor here being that each transducer up to the limit n has a corresponding switch for input, again up to the limit n. n, the number of transducers and n, the number of switches being the same number.

15. According to Claims 11 to 14, whereby the microcomputer is programmed such that the manual input means can be made to function such that any switch on the manual input device can correspond to more than one transducer in a pre-determined arrangement. The only limiting factor here being the mathematically possible combinations of n. n being the number of transducers as well as the number of switches.

16. According to Claims 1 to 15. All switching relayed through the transducers in any of the aforementioned embodiments whereby the signal processing is of an audio nature can simultaneously be relayed through the transducers of a type necessary for the control of lighting systems and effects, as well as transducers of the type necessary for the control of visual effects, whether projected onto a screen, as in a cinema, broadcast over the airwaves as in terrestrial television, or broadcast via communications satellite, as in satellite television, or relayed through a video recorder, as in the case of pre-recorded television, or relayed through a microcomputer, as in the case of any pre-recorded audio-visual information where it is necessary for a microcomputer to interpret the information from the code in which it has been programmed for storage.

Patents Act 1977 Examiner's report to the Comptroller under Section 17 (The Search report) -21-	Application number GB 9309378.9
Relevant Technical Fields (i) UK Cl (Ed.L) H4R: RSAD, RSX, RSS (ii) Int Cl (Ed.5) H04R	Search Examiner MR S SATKURUNATH Date of completion of Search 27 JULY 1994
Databases (see below) (i) UK Patent Office collections of GB, EP, WO and US patent specifications. (ii) ONLINE DATABASES: WPI, JAPIO, EDOC	Documents considered relevant following a search in respect of Claims :- 1-16

Categories of documents

X:	Document indicating lack of novelty or of inventive step.	**P:**	Document published on or after the declared priority date but before the filing date of the present application.
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A:	Document indicating technological background and/or state of the art.	**&:**	Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages	Relevant to claim(s)
X	WPI Abstract Accession No. 84-159346 (26) and DE 3246896 A (OCHSENKUHN) 20.06.84 (see abstract)	1-4, 10
X	WPI Abstract Accession No. 75-C3314W (09) and DE 2341342 A (WERNER) 20.02.75 (see abstract)	1-4, 10

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